CORRECTION

Correction to: A novel FPGA-based testbench framework for SDI stream verification

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The original article can be found online at https://doi.org/10.1186/ s13640-020-00515-5.

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Correction to: J Image Video Proc 2020, 31 (2020) https://doi.org/10.1186/s13640-020-00515-5

Following publication of the original article [1], the authors identified a few errors in the published article.

- 1. Body text contains incorrect sentence in a simulation, it is possible to analyze the different frequency rates, but it is missing a test generator able to communicate with transceiver. It should be corrected to in a simulation, it is possible to analyze the different frequency rates, but it is missing a test generator able to communicate with the DUT through the transceiver
- 2. The Figs. 11 and 12 had been inverted. Correct Figs. 11 and 12 with captions should look as per below:

The original article [1] has been corrected.

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Options Window	
Status	
Format	(1280 x 720) 50p
Digital Input	Wrong Formet
Motion Content	-
Luminance Content	-
Chrominance Content	-
Analog Sync	Missing
Closed Caption	
ANC 608	-
ANC 708	-
Error Checking	
YCbCr Range Check	00000000
RGB Range Check	04075186
TRS Check	00029174
LINE Check	00376826
CRC Check	00000000
ANC Check	00000000
Time Code Error Checking	
ATC Stuck Frames	00000000
ATC Skipped Frames	00000000
Time Codes	
ATC (Source: VITC #1)	
ig. 11 Output from the Omnitek video analyzer	



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